# **CPI2-GDMR Relay Demultiplexer**

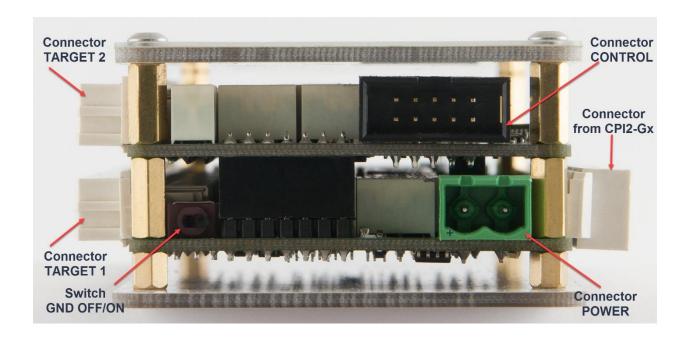
CPI2-GDMR relay demultiplexer shown on the picture below is used for:

- a) doubling a number of CPI2-Gx' device programmer channels for sequential device programming and
- b) disconnecting the device programmer from the target panel while it is under functional testing.

The demultiplexer uses miniature electromechanical relays for switching Digital IO signal lines (7 sites by 12 signals in each) plus GND (ground) lines (7 sites by 9 GND signals in each). Each programming site can be controlled individually.



A CPI2-GDMR unit should be powered from an external 12 to 18V@2A power supply. The unit has a couple of two-pin green power connectors to plug a cable or wires from the power adapter, which can be connected to either side, wherever it is more convenient. These connectors are located on both short end faces of the CPI2-GDMR unit. See the CPI2-GDMR side view below.

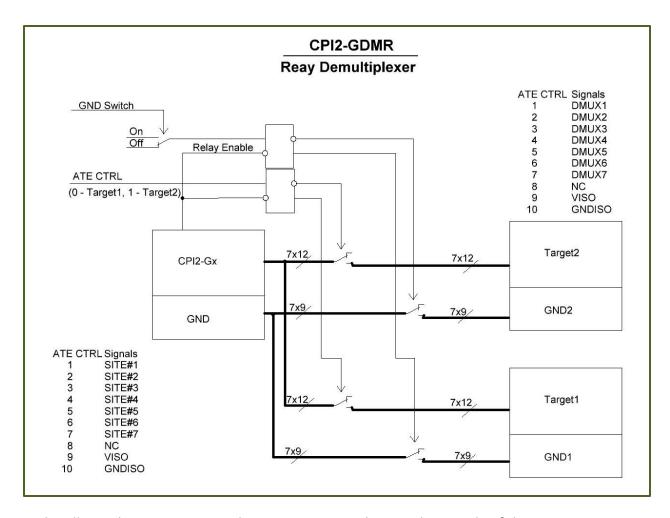


A CPI2-GDMR unit docs to female type **TARGET – channel A** or **TARGET – channel B** 150-pin DIN connectors installed on CPI2-Gx device programmers by a male type complimentary connector marked on the top label as **CPI2-Gx Device Programmer**. This connector locates on a long rear side of the CPI2-GDMR unit.

It is possible to dock two relay demultiplexers to both **A** and **B** channel connectors – in this case the total number of programming channels will be quadrupled. [Note: CPI2-Gx device programmers belonging to the revision #1 with serial numbers GMV-1xxxxxx do not allow demultiplexing the **B** channel by CPI2-GDMR!].

On an opposite, front site a CPI2-GDMR unit has a pair of female type 150-pin DIN connectors marked as **TARGET 1 (Bottom)** and **TARGET 2 (Top)**. The demultiplexer toggles ISP lines between these two connectors but the signals come to the panels for short periods of time while the CPI2-Gx programs, reads or maintains other operations on the DUTs installed on the target panel. Most of the time relays keep the ISP lines disconnected from the programmer.

See the CPI2-GDMR flowchart below.



In the idle mode a CPI2-Gx gang device programmer keeps relays inside of the CPI2-GDMR unit inactive, so the ISP signals and ground lines coming from the CPI2-Gx device programmer remain disconnected from the target panel and ATE lines. In this mode the target panel remains disconnected from the programmer; most likely in this stage the panel is under functional testing. Only when the programmer operates on the target panel, i.e. it executes an **Auto Program** batch of command it issues the **Relay Enable** signal that switches relays on and connects ISP signals and ground lines to the target.

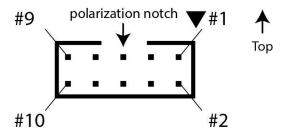
The demultiplexer enables two modes for switching ground lines between the programmer and target:

- **GND ON** when the ground lines on the CPI2-Gx TARGET connector remain always connected to the ground circuit of the target, even while the relays disconnect ISP signals from the target panel;
- **GND OFF** when the CPI2-Gx ground lines are disconnected synchronously with the ISP signals and remains disconnected between executing **Auto Program** batch of command.

Switching between the **GND ON** and **GND OFF** modes is controlled manually by a miniature switch located on one side of the unit and marked on the top of the CPI2-GTRB unit as **GND/ON-OFF**.

#### **Connector CONTROL**

The signals that drive toggling between the **TARGET 1** and **TARGET 2** connectors come from the ATE to the 10-pin connector marked as **CTRL** on a top of the demultiplexer unit. This connector is located on one of the short end faces of the CPI2-GDMR unit. See the connector pinout below):



Here is the corresponding signal table:

CTRL pin#	Signal from ATE	Site# to control or description
1	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#1 or DMUX1
2	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#2 or DMUX2
3	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#3 or DMUX3
4	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#4 or DMUX4
5	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#5 or DMUX5
6	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#6 or DMUX6
7	If =0, switch to TARGET 1, if =1 – TARGET 2	Site#7 or DMUX7
8	Not used	Not used
9	VISO	Galvanically isolated voltage 5V
10	GNDISO	Galvanically isolated GND

Each programming site from #1 to #7 can be toggled between **TARGET 1** and **TARGET 2** connectors individually. To toggle all them synchronously by a single signal via a single wire it is necessary to join the control pins #1 to #7.

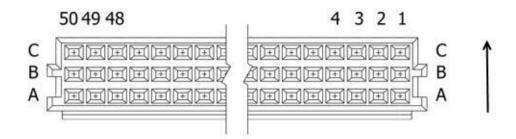
By default, these CTRL pins #1 to #7 are pulled down to log. 0. So, by default, when ATE does not generate any signals on the pin#1 ..7, the programmer is connected to the **TARGET 1**. Setting log. 1 on a certain CTRL pin toggle the site to the **TARGET 2**.

The **CTRL** connector outputs a galvanically isolated signal with the log. 1 level to the pin# 9 (VISO). This signal can be used for switching the programmer from the **TARGET 1** to **TARGET 2** by connecting the pin# 9 to an appropriate pin#1 ..7. If the pin# 9 is connected to all pins#1 to #7 then all programming sites will be switched to the **TARGET 2**.

Connecting the CPI2-Gx device programmer to either **TARGET 1** or **TARGET 2** is enabled *only* while the programmer conducts any programming operation (see the **Relay Enable** signal in the CPI2-GDMR flowchart). In between of the programming operations all the relays disconnect the programmer from the target. Therefore, stopping the programming session allows to provide the target panel functional testing or other manipulations without influence of the Phyton equipment.

#### **Connectors TARGET**

A CPI2-GDMR relay demultiplexer unit has three 150-pin connectors – an "input" one located on the side docking to a CPI2-Gx gang programmer and a pair of "output" connectors: **TARGET 1** and **TARGET 2** that connect target panel with DUTs. All three connectors are the same type 150-pin DIN connectors with the following pinout:



The matrix below shows ISP signal and GND pinouts of **TARGET - channel A** and **TARGET - channel B** "input" connectors on a side docking to a CPI2-Gx device programmer. Both connectors have identical pinouts.

**TARGET - channel A** 

Pin#	Pin Name	Description	Pin#	Pin Name	Description	Pin#	Pin Name	Description
A1	1/PA1	Site1: digital IO pin1	B1	GND	Ground	C1	1/PA7	Site1: digital IO pin7
A2	1/PA2	Site1: digital IO pin2	B2	GND	Ground	C2	1/PA8	Site1: digital IO pin8
А3	1/PA3	Site1: digital IO pin3	В3	GND	Ground	C3	1/PA9	Site1: digital IO pin9
A4	1/PA4	Site1: digital IO pin4	В4	GND	Ground	C4	1/PA10	Site1: digital IO pin10
A5	1/PA5	Site1: digital IO pin5	В5	GND	Ground	C5	1/PA11	Site1: digital IO pin11
A6	1/PA6	Site1: digital IO pin6	В6	GND	Ground	C6	1/PA12	Site1: digital IO pin12
Α7	DNU	Reserved for Phyton use*	В7	GND	Ground	<b>C7</b>	DNU	Reserved for Phyton use*
A8	2/PA1	Site2: digital IO pin1	В8	GND	Ground	C8	2/PA7	Site2: digital IO pin7
A9	2/PA2	Site2: digital IO pin2	В9	GND	Ground	C9	2/PA8	Site2: digital IO pin8
A10	2/PA3	Site2: digital IO pin3	B10	GND	Ground	C10	2/PA9	Site2: digital IO pin9
A11	2/PA4	Site2: digital IO pin4	B11	GND	Ground	C11	2/PA10	Site2: digital IO pin10
A12	2/PA5	Site2: digital IO pin5	B12	GND	Ground	C12	2/PA11	Site2: digital IO pin11
A13	2/PA6	Site2: digital IO pin6	B13	GND	Ground	C13	2/PA12	Site2: digital IO pin12
A14	DNU	Reserved for Phyton use*	B14	GND	Ground	C14	DNU	Reserved for Phyton use*
A15	3/PA1	Site3: digital IO pin1	B15	GND	Ground	C15	3/PA7	Site3: digital IO pin7
A16	3/PA2	Site3: digital IO pin2	B16	GND	Ground	C16	3/PA8	Site3: digital IO pin8
A17	3/PA3	Site3: digital IO pin3	B17	GND	Ground	C17	3/PA9	Site3: digital IO pin9
A18	3/PA4	Site3: digital IO pin4	B18	GND	Ground	C18	3/PA10	Site3: digital IO pin10
A19	3/PA5	Site3: digital IO pin5	B19	GND	Ground	C19	3/PA11	Site3: digital IO pin11
A20	3/PA6	Site3: digital IO pin6	B20	GND	Ground	C20	3/PA12	Site3: digital IO pin12
A21	DNU	Reserved for Phyton use*	B21	GND	Ground	C21	DNU	Reserved for Phyton use*
A22	GND	Ground	B22	GND	Ground	C22	GND	Ground

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A23	4/PA1	Site4: digital IO pin1	B23	GND	Ground	C23	4/PA7	Site4: digital IO pin7
A24	4/PA2	Site4: digital IO pin2	B24	GND	Ground	C24	4/PA8	Site4: digital IO pin8
A25	4/PA3	Site4: digital IO pin3	B25	GND	Ground	C25	4/PA9	Site4: digital IO pin9
A26	4/PA4	Site4: digital IO pin4	B26	GND	Ground	C26	4/PA10	Site4: digital IO pin10
A27	4/PA5	Site4: digital IO pin5	B27	GND	Ground	C27	4/PA11	Site4: digital IO pin11
A28	4/PA6	Site4: digital IO pin6	B28	GND	Ground	C28	4/PA12	Site4: digital IO pin12
A29	DNU	Reserved for Phyton use*	B29	GND	Ground	C29	DNU	Reserved for Phyton use*
A30	DNU	Reserved for Phyton use*	B30	GND	Ground	C30	DNU	Reserved for Phyton use*
A31	5/PA1	Site5: digital IO pin1	B31	GND	Ground	C31	5/PA7	Site5: digital IO pin7
A32	5/PA2	Site5: digital IO pin2	B32	GND	Ground	C32	5/PA8	Site5: digital IO pin8
A33	5/PA3	Site5: digital IO pin3	B33	GND	Ground	C33	5/PA9	Site5: digital IO pin9
A34	5/PA4	Site5: digital IO pin4	B34	GND	Ground	C34	5/PA10	Site5: digital IO pin10
A35	5/PA5	Site5: digital IO pin5	B35	GND	Ground	C35	5/PA11	Site5: digital IO pin11
A36	5/PA6	Site5: digital IO pin6	B36	GND	Ground	C36	5/PA12	Site5: digital IO pin12
A37	DNU	Reserved for Phyton use*	B37	GND	Ground	C37	DNU	Reserved for Phyton use*
A38	6/PA1	Site6: digital IO pin1	B38	GND	Ground	C38	6/PA7	Site6: digital IO pin7
A39	6/PA2	Site6: digital IO pin2	B39	GND	Ground	C39	6/PA8	Site6: digital IO pin8
A40	6/PA3	Site6: digital IO pin3	B40	GND	Ground	C40	6/PA9	Site6: digital IO pin9
A41	6/PA4	Site6: digital IO pin4	B41	GND	Ground	C41	6/PA10	Site6: digital IO pin10
A42	6/PA5	Site6: digital IO pin5	B42	GND	Ground	C42	6/PA11	Site6: digital IO pin11
A43	6/PA6	Site6: digital IO pin6	B43	GND	Ground	C43	6/PA12	Site6: digital IO pin12
A 4 4								
A44	DNU	Reserved for Phyton use*	B44	GND	Ground	C44	DNU	Reserved for Phyton use*
A44 A45	DNU 7/PA1	Reserved for Phyton use* Site7: digital IO pin1	B44 B45	GND GND	Ground Ground	C44 C45	DNU 7/PA7	Reserved for Phyton use* Site7: digital IO pin7
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A45	7/PA1	Site7: digital IO pin1	B45	GND	Ground	C45	7/PA7	Site7: digital IO pin7
A45 A46	7/PA1 7/PA2	Site7: digital IO pin1 Site7: digital IO pin2	B45 B46	GND GND	Ground Ground	C45 C46	7/PA7 7/PA8	Site7: digital IO pin7 Site7: digital IO pin8
A45 A46 A47	7/PA1 7/PA2 7/PA3	Site7: digital IO pin1 Site7: digital IO pin2 Site7: digital IO pin3	B45 B46 B47	GND GND GND	Ground Ground Ground	C45 C46 C47	7/PA7 7/PA8 7/PA9	Site7: digital IO pin7 Site7: digital IO pin8 Site7: digital IO pin9
A45 A46 A47 A48	7/PA1 7/PA2 7/PA3 7/PA4	Site7: digital IO pin1 Site7: digital IO pin2 Site7: digital IO pin3 Site7: digital IO pin4	B45 B46 B47 B48	GND GND GND GND	Ground Ground Ground	C45 C46 C47 C48	7/PA7 7/PA8 7/PA9 7/PA10	Site7: digital IO pin7 Site7: digital IO pin8 Site7: digital IO pin9 Site7: digital IO pin10

# TARGET - channel B

Pin#	Pin Name	Description	Pin #	Pin Name	Description	Pin #	Pin Name	Description
A50	1/PB1	Site1: digital IO pin1	B50	GND	Ground	C50	1/PB7	Site1: digital IO pin7
A49	1/PB2	Site1: digital IO pin2	B49	GND	Ground	C49	1/PB8	Site1: digital IO pin8
A48	1/PB3	Site1: digital IO pin3	B48	GND	Ground	C48	1/PB9	Site1: digital IO pin9
A47	1/PB4	Site1: digital IO pin4	B47	GND	Ground	C47	1/PB10	Site1: digital IO pin10
A46	1/PB5	Site1: digital IO pin5	B46	GND	Ground	C46	1/PB11	Site1: digital IO pin11
A45	1/PB6	Site1: digital IO pin6	B45	GND	Ground	C45	1/PB12	Site1: digital IO pin12
A44	DNU	Reserved for Phyton use*	B44	GND	Ground	C44	DNU	Reserved for Phyton use*
A43	2/PB1	Site2: digital IO pin1	B43	GND	Ground	C43	2/PB7	Site2: digital IO pin7
A42	2/PB2	Site2: digital IO pin2	B42	GND	Ground	C42	2/PB8	Site2: digital IO pin8
A41	2/PB3	Site2: digital IO pin3	B41	GND	Ground	C41	2/PB9	Site2: digital IO pin9
A40	2/PB4	Site2: digital IO pin4	B40	GND	Ground	C40	2/PB10	Site2: digital IO pin10
A39	2/PB5	Site2: digital IO pin5	B39	GND	Ground	C39	2/PB11	Site2: digital IO pin11
A38	2/PB6	Site2: digital IO pin6	B38	GND	Ground	C38	2/PB12	Site2: digital IO pin12
A37	DNU	Reserved for Phyton use*	B37	GND	Ground	C37	DNU	Reserved for Phyton use*
A36	3/PB1	Site3: digital IO pin1	B36	GND	Ground	C36	3/PB7	Site3: digital IO pin7

A35	3/PB2	Site3: digital IO pin2	B35	GND	Ground	C35	3/PB8	Site3: digital IO pin8
A34	3/PB3	Site3: digital IO pin3	B34	GND	Ground	C34	3/PB9	Site3: digital IO pin9
A33	3/PB4	Site3: digital IO pin4	B33	GND	Ground	C33	3/PB10	Site3: digital IO pin10
A32	3/PB5	Site3: digital IO pin5	B32	GND	Ground	C32	3/PB11	Site3: digital IO pin11
A31	3/PB6	Site3: digital IO pin6	B31	GND	Ground	C31	3/PB12	Site3: digital IO pin12
A30	DNU	Reserved for Phyton use*	B30	GND	Ground	C30	DNU	Reserved for Phyton use*
A29	GND	Ground	B29	GND	Ground	C29	GND	Ground
A28	4/PB1	Site4: digital IO pin1	B28	GND	Ground	C28	4/PB7	Site4: digital IO pin7
A27	4/PB2	Site4: digital IO pin2	B27	GND	Ground	C27	4/PB8	Site4: digital IO pin8
A26	4/PB3	Site4: digital IO pin3	B26	GND	Ground	C26	4/PB9	Site4: digital IO pin9
A25	4/PB4	Site4: digital IO pin4	B25	GND	Ground	C25	4/PB10	Site4: digital IO pin10
A24	4/PB5	Site4: digital IO pin5	B24	GND	Ground	C24	4/PB11	Site4: digital IO pin11
A23	4/PB6	Site4: digital IO pin6	B23	GND	Ground	C23	4/PB12	Site4: digital IO pin12
A22	DNU	Reserved for Phyton use*	B22	GND	Ground	C22	DNU	Reserved for Phyton use*
A21	DNU	Reserved for Phyton use*	B21	GND	Ground	C21	DNU	Reserved for Phyton use*
A20	5/PB1	Site5: digital IO pin1	B20	GND	Ground	C20	5/PB7	Site5: digital IO pin7
A19	5/PB2	Site5: digital IO pin2	B19	GND	Ground	C19	5/PB8	Site5: digital IO pin8
A18	5/PB3	Site5: digital IO pin3	B18	GND	Ground	C18	5/PB9	Site5: digital IO pin9
A17	5/PB4	Site5: digital IO pin4	B17	GND	Ground	C17	5/PB10	Site5: digital IO pin10
A16	5/PB5	Site5: digital IO pin5	B16	GND	Ground	C16	5/PB11	Site5: digital IO pin11
A15	5/PB6	Site5: digital IO pin6	B15	GND	Ground	C15	5/PB12	Site5: digital IO pin12
A14	DNU	Reserved for Phyton use*	B14	GND	Ground	C14	DNU	Reserved for Phyton use*
A13	6/PB1	Site6: digital IO pin1	B13	GND	Ground	C13	6/PB7	Site6: digital IO pin7
A12	6/PB2	Site6: digital IO pin2	B12	GND	Ground	C12	6/PB8	Site6: digital IO pin8
A11	6/PB3	Site6: digital IO pin3	B11	GND	Ground	C11	6/PB9	Site6: digital IO pin9
A10	6/PB4	Site6: digital IO pin4	B10	GND	Ground	C10	6/PB10	Site6: digital IO pin10
A9	6/PB5	Site6: digital IO pin5	В9	GND	Ground	C9	6/PB11	Site6: digital IO pin11
A8	6/PB6	Site6: digital IO pin6	В8	GND	Ground	C8	6/PB12	Site6: digital IO pin12
A7	DNU	Reserved for Phyton use*	В7	GND	Ground	С7	DNU	Reserved for Phyton use*
A6	7/PB1	Site7: digital IO pin1	В6	GND	Ground	C6	7/PB7	Site7: digital IO pin7
A5	7/PB2	Site7: digital IO pin2	В5	GND	Ground	C5	7/PB8	Site7: digital IO pin8
A4	7/PB3	Site7: digital IO pin3	В4	GND	Ground	C4	7/PB9	Site7: digital IO pin9
А3	7/PB4	Site7: digital IO pin4	В3	GND	Ground	C3	7/PB10	Site7: digital IO pin10
A2	7/PB5	Site7: digital IO pin5	B2	GND	Ground	C2	7/PB11	Site7: digital IO pin11
A1	7/PB6	Site7: digital IO pin6	B1	GND	Ground	C1	7/PB12	Site7: digital IO pin12

The matrix below shows ISP signal and GND pinouts of **TARGET 1** and **TARGET 2** "output" connectors installed on a CPI2-GDMR relay demultiplexer unit. Both connectors have identical pinouts.

# **TARGET 1 and TARGET 2 output connectors**

Pin #	Pin Name	Description	Pin #	Pin Name	Description	Pin #	Pin Name	Description
A1	1/PA1	Site1: digital IO pin1	B1	1/GND	Site#1 Ground	C1	1/PA7	Site1: digital IO pin7
A2	1/PA2	Site1: digital IO pin2	B2	1/GND	Site#1 Ground	C2	1/PA8	Site1: digital IO pin8
А3	1/PA3	Site1: digital IO pin3	В3	1/GND	Site#1 Ground	С3	1/PA9	Site1: digital IO pin9

A4	1/PA4	Site1: digital IO pin4	В4	1/GND	Site#1 Ground	C4	1/PA10	Site1: digital IO pin10
A5	1/PA5	Site1: digital IO pin5	B5	1/GND	Site#1 Ground	C5	1/PA11	Site1: digital IO pin11
A6	1/PA6	Site1: digital IO pin6	В6	1/GND	Site#1 Ground	C6	1/PA12	Site1: digital IO pin12
A7	DNU	Reserved for Phyton use*	В7	1/GND	Site#1 Ground	<b>C7</b>	DNU	Reserved for Phyton use*
A8	2/PA1	Site2: digital IO pin1	В8	2/GND	Site#2 Ground	C8	2/PA7	Site2: digital IO pin7
A9	2/PA2	Site2: digital IO pin2	В9	2/GND	Site#2 Ground	С9	2/PA8	Site2: digital IO pin8
A10	2/PA3	Site2: digital IO pin3	B10	2/GND	Site#2 Ground	C10	2/PA9	Site2: digital IO pin9
A11	2/PA4	Site2: digital IO pin4	B11	2/GND	Site#2 Ground	C11	2/PA10	Site2: digital IO pin10
A12	2/PA5	Site2: digital IO pin5	B12	2/GND	Site#2 Ground	C12	2/PA11	Site2: digital IO pin11
A13	2/PA6	Site2: digital IO pin6	B13	2/GND	Site#2 Ground	C13	2/PA12	Site2: digital IO pin12
A14	DNU	Reserved for Phyton use*	B14	2/GND	Site#2 Ground	C14	DNU	Reserved for Phyton use*
A15	3/PA1	Site3: digital IO pin1	B15	3/GND	Site#3 Ground	C15	3/PA7	Site3: digital IO pin7
A16	3/PA2	Site3: digital IO pin2	B16	3/GND	Site#3 Ground	C16	3/PA8	Site3: digital IO pin8
A17	3/PA3	Site3: digital IO pin3	B17	3/GND	Site#3 Ground	C17	3/PA9	Site3: digital IO pin9
A18	3/PA4	Site3: digital IO pin4	B18	3/GND	Site#3 Ground	C18	3/PA10	Site3: digital IO pin10
A19	3/PA5	Site3: digital IO pin5	B19	3/GND	Site#3 Ground	C19	3/PA11	Site3: digital IO pin11
A20	3/PA6	Site3: digital IO pin6	B20	3/GND	Site#3 Ground	C20	3/PA12	Site3: digital IO pin12
A21	DNU	Reserved for Phyton use*	B21	3/GND	Site#3 Ground	C21	DNU	Reserved for Phyton use*
A22	3/GND	Site#3 Ground	B22	3/GND	Site#3 Ground	C22	3/GND	Site#3 Ground
A23	4/PA1	Site4: digital IO pin1	B23	4/GND	Site#4 Ground	C23	4/PA7	Site4: digital IO pin7
A24	4/PA2	Site4: digital IO pin2	B24	4/GND	Site#4 Ground	C24	4/PA8	Site4: digital IO pin8
A25	4/PA3	Site4: digital IO pin3	B25	4/GND	Site#4 Ground	C25	4/PA9	Site4: digital IO pin9
A26	4/PA4	Site4: digital IO pin4	B26	4/GND	Site#4 Ground	C26	4/PA10	Site4: digital IO pin10
A27	4/PA5	Site4: digital IO pin5	B27	4/GND	Site#4 Ground	C27	4/PA11	Site4: digital IO pin11
A28	4/PA6	Site4: digital IO pin6	B28	4/GND	Site#4 Ground	C28	4/PA12	Site4: digital IO pin12
A29	DNU	Reserved for Phyton use*	B29	4/GND	Site#4 Ground	C29	DNU	Reserved for Phyton use*
A30	DNU	Reserved for Phyton use*	B30	5/GND	Site#5 Ground	C30	DNU	Reserved for Phyton use*
A31	5/PA1	Site5: digital IO pin1	B31	5/GND	Site#5 Ground	C31	5/PA7	Site5: digital IO pin7
A32	5/PA2	Site5: digital IO pin2	B32	5/GND	Site#5 Ground	C32	5/PA8	Site5: digital IO pin8
A33	5/PA3	Site5: digital IO pin3	B33	5/GND	Site#5 Ground	C33	5/PA9	Site5: digital IO pin9
A34	5/PA4	Site5: digital IO pin4	B34	5/GND	Site#5 Ground	C34	5/PA10	Site5: digital IO pin10
A35	5/PA5	Site5: digital IO pin5	B35	5/GND	Site#5 Ground	C35	5/PA11	Site5: digital IO pin11
A36	5/PA6	Site5: digital IO pin6	B36	5/GND	Site#5 Ground	C36	5/PA12	Site5: digital IO pin12
A37	DNU	Reserved for Phyton use*	B37	6/GND	Site#6 Ground	C37	DNU	Reserved for Phyton use*
A38	6/PA1	Site6: digital IO pin1	B38	6/GND	Site#6 Ground	C38	6/PA7	Site6: digital IO pin7
A39	6/PA2	Site6: digital IO pin2	B39	6/GND	Site#6 Ground	C39	6/PA8	Site6: digital IO pin8
A40	6/PA3	Site6: digital IO pin3	B40	6/GND	Site#6 Ground	C40	6/PA9	Site6: digital IO pin9
A41	6/PA4	Site6: digital IO pin4	B41	6/GND	Site#6 Ground	C41	6/PA10	Site6: digital IO pin10
A42	6/PA5	Site6: digital IO pin5	B42	6/GND	Site#6 Ground	C42	6/PA11	Site6: digital IO pin11
A43	6/PA6	Site6: digital IO pin6	B43	6/GND	Site#6 Ground	C43	6/PA12	Site6: digital IO pin12
A44	DNU	Reserved for Phyton use*	B44	7/GND	Site#7 Ground	C44	DNU	Reserved for Phyton use*
A45	7/PA1	Site7: digital IO pin1	B45	7/GND	Site#7 Ground	C45	7/PA7	Site7: digital IO pin7
A46	7/PA2	Site7: digital IO pin2	B46	7/GND	Site#7 Ground	C46	7/PA8	Site7: digital IO pin8
A47	7/PA3	Site7: digital IO pin3	B47	7/GND	Site#7 Ground	C47	7/PA9	Site7: digital IO pin9
A48	7/PA4	Site7: digital IO pin4	B48	7/GND	Site#7 Ground	C48	7/PA10	Site7: digital IO pin10
A49	7/PA5	Site7: digital IO pin5	B49	7/GND	Site#7 Ground	C49	7/PA11	Site7: digital IO pin11
A50	7/PA6	Site7: digital IO pin6	B50	7/GND	Site#7 Ground	C50	7/PA12	Site7: digital IO pin12

#### Where:

- Signals marked as DNU Reserved for Phyton use\*, may not be used by CPI2-GDMR demultiplexer users. These connector pins should be left untouched.
- Site#/PAn and Site#/PBn (n=1...10) logical signals formed by high-speed buffers that can output target-specific logic 0 or 1, Vcc or GND levels, according to the chosen target device type. The buffers are bidirectional, also serving as inputs when the programmer reads data.
- Site#/PAm and Site#/PBm (m=11 & 12) signals formed by high speed mixed-signal circuits that can also output target-specific logic 0 or 1, Vpp or GND levels according to the type of the chosen target device. These lines can output Vcc with levels from 1.2 to 5.5V @ up to 350mA. The mixed-signal buffers are bidirectional, also serving as inputs when the <%CPN%> programmer reads data. In addition, these two signals can output Vpp voltage with levels from 1.5V to 15V @ up to 100mA.

In general, ISP signals and GND line map remains the same for the **TARGET 1** and **TARGET 2** connectors that replicate status of the device programmer depending on what **TARGET** is active: **1** or **2**. The major difference is that all GND lines on an output connector **TARGET** are galvanically connected while the GND lines on the **TARGET 1** and **TARGET 2** connectors are separated in seven groups (Site#1 Ground, Site#2 Ground, etc.) that allows to control each site from #1 to #7 individually.